MICROPROCESSORS AND INTERFACING

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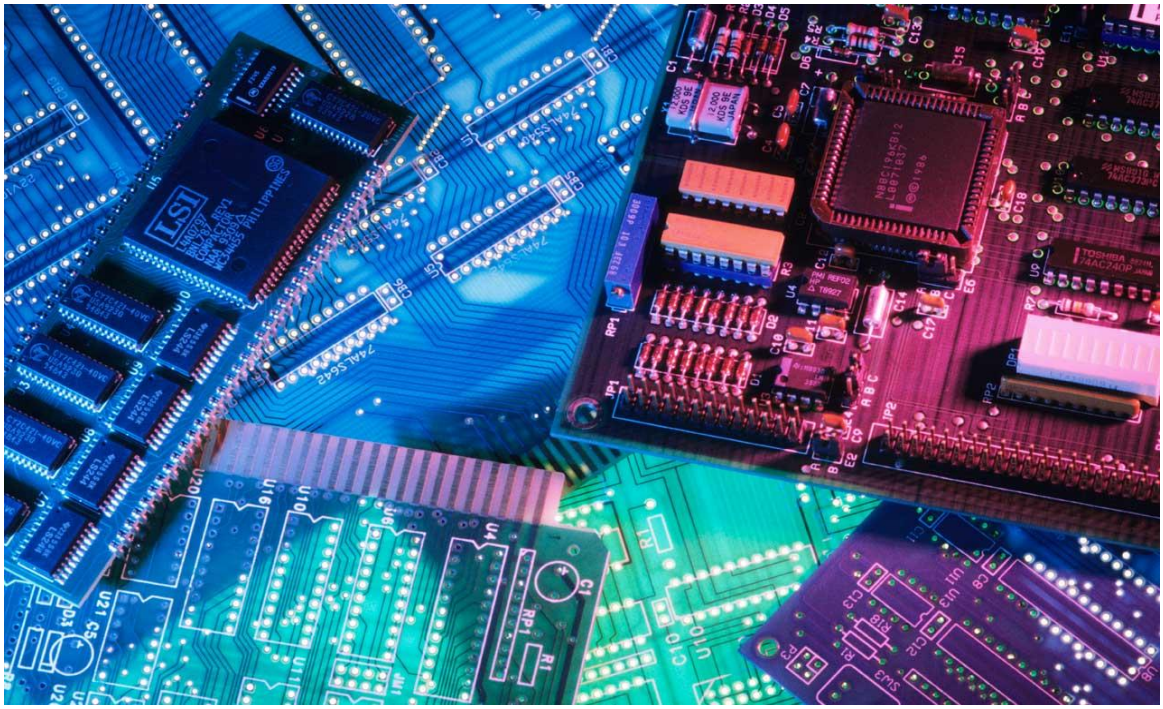

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UNIT – I
8085 MICROPROCESSOR

History of Microprocessors, Introduction to 8085, pin description, Architecture, bus timing and instruction timing, flag register, de-multiplexing of buses, generation of control signals, Addressing modes, interrupts.

INDEX

UNIT – I
8085 MICROPROCESSOR

INTRODUCTION TO MICROPROCESSORS

Microprocessor is an IC which has only the CPU inside them i.e. only the processing powers such as Intel's Pentium 1,2,3,4, core 2 duo, i3, i5 etc. These microprocessors don't have RAM, ROM, and other peripheral on the chip. A system designer has to add them externally to make them functional. Application of microprocessor includes Desktop PC's, Laptops, notepads etc.

Microprocessor find applications where tasks are unspecific like developing software, games, websites, photo editing, creating documents etc. In such cases the relationship between input and output is not defined. They need high amount of resources like RAM, ROM, I/O ports etc. The clock speed of the Microprocessor is quite high as compared to the microcontroller. Whereas the microcontrollers operate from a few MHz to 30 to 50 MHz, today's microprocessor operate above 1GHz as they perform complex tasks.

Definition: Microprocessor is a multipurpose, programmable, register based electronic device which read binary instructions from memory, processes the input data as per instructions and provides output.

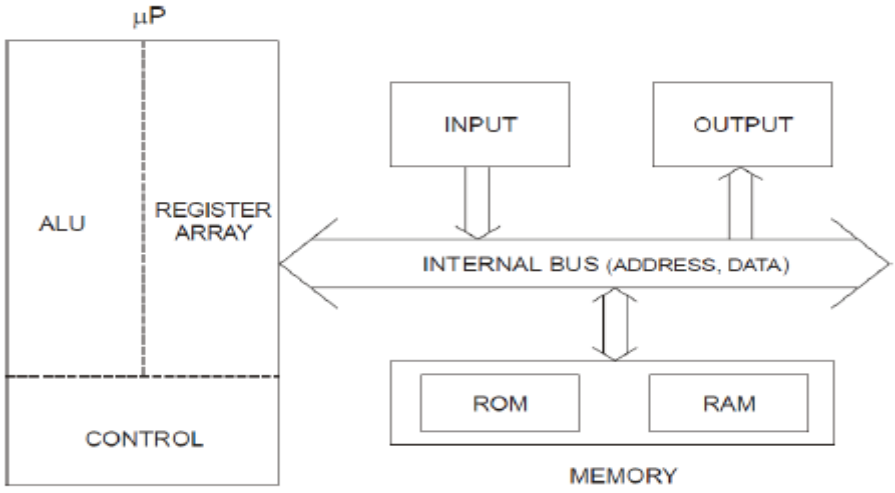

Figure: Block diagram of microprocessor

General features:

1. Do not have inbuilt RAM or ROM and timer.
2. Input and output ports are not available, requires extra device like 8155/8255
3. Do not have inbuilt serial port, requires 8250/8251 device.
4. Program and data are stored in same memory.
5. Less multifunction pins on IC.
6. Boolean operation is not possible directly.
7. It takes many instructions to read and write data from external memory.

HISTORY OF MICROPROCESSORS

Evolution of Microprocessors:

We can categorize the microprocessor according to the generations or according to the size of the microprocessor:

First Generation (4 - bit Microprocessors):

The first generation microprocessors were introduced in the year 1971-1972 by Intel Corporation. It was named **Intel 4004** since it was a 4-bit processor. It was a processor on a single chip. It could perform simple arithmetic and logical operations such as addition, subtraction, Boolean OR and Boolean AND. It had a control unit capable of performing control functions like fetching an instruction from storage memory, decoding it, and then generating control pulses to execute it.

Second Generation (8 - bit Microprocessor):

The second generation microprocessors were introduced in 1973 again by Intel. It was a first 8 - bit microprocessor which could perform arithmetic and logic operations on 8-bit words. It was **Intel 8008**, and another improved version was **Intel 8080.**

Third Generation (16 - bit Microprocessor):

The third generation microprocessors, introduced in 1978 were represented by **Intel's 8086, 8088, Zilog Z800 and 80286**, which were 16 - bit processors with a performance like minicomputers.

Fourth Generation (32 - bit Microprocessors):

Several different companies introduced the 32-bit microprocessors, but the most popular one is the **Intel 80386**.

Fifth Generation (64 - bit Microprocessors):

From 1995 to now we are in the fifth generation. After 80856, Intel came out with a new processor namely Pentium processor followed by **Pentium Pro CPU, Intel Core, i3, i5, i7** which allows multiple CPUs in a single system to achieve multiprocessing.

Basic Terms used in Microprocessor:

Here is a list of some basic terms used in microprocessor:

Bus - Set of conductors intended to transmit data, address or control information to different elements in a microprocessor. A microprocessor will have three types of buses, i.e., data bus, address bus, and control bus.

Clock Speed - It is the number of operations per second the processor can perform. It can be expressed in megahertz (MHz) or gigahertz (GHz). It is also called the Clock Rate.

Instruction Set - The group of commands that the microprocessor can understand is called Instruction set. It is an interface between hardware and software.

IPC (Instructions per Cycle) - It is a measure of how many instructions a CPU is capable of executing in a single clock.

Features of Microprocessor:

1) **Low Cost** - Due to integrated circuit technology microprocessors are available at very low cost. It will reduce the cost of a computer system.

2) **High Speed** - Due to the technology involved in it, the microprocessor can work at very high speed. It can execute millions of instructions per second.

3) **Small Size** - A microprocessor is fabricated in a very less footprint due to very large scale and ultra large scale integration technology. Because of this, the size of the computer system is reduced.

4) **Versatile** - The same chip can be used for several applications, therefore, microprocessors are versatile.

5) **Low Power Consumption** - Microprocessors are using metal oxide semiconductor technology, which consumes less power.

6) **Less Heat Generation** - Microprocessors uses semiconductor technology which will not emit much heat as compared to vacuum tube devices.

7) **Reliable** - Since microprocessors use semiconductor technology, therefore, the failure rate is very less. Hence it is very reliable.

8) **Portable** - Due to the small size and low power consumption microprocessors are portable.

INTRODUCTION TO 8085

The salient features of 8085 microprocessor are:

1) It is an 8 bit microprocessor
2) It is manufactured with N-MOS technology.
3) It has 16-bit address bus and hence can address up to 2^{16} =65536 bytes (64KB) memory locations through A_0-A_{15}.
4) The first 8 lines of address bus and 8 lines of data bus are multiplexed $AD_0 – AD_7$.
5) Data bus is a group of 8 lines $D_0 – D_7$.
6) It supports external interrupt request.
7) A 16 bit program counter (PC)
8) A 16 bit stack pointer (SP)
9) Six 8-bit general purpose register arranged in pairs: BC, DE, HL.
10) It requires a signal +5V power supply and operates at 3.2 MHZ single phase clock.
11) It is enclosed with 40 pins DIP (Dual in line package).

PIN DESCRIPTION OF 8085

Features:

1) It is an 8-bit microprocessor
2) Manufactured with N-MOS technology
3) 40 pin IC package
4) It has 16-bit address bus and thus has 2^{16} = 64 KB addressing capability.
5) Operate with 3 MHz single-phase clock
6) +5 V single power supply

The logic pin layout and signal groups of the 8085 microprocessor are shown in below figure. All the signals are classified into seven groups:

1) Address bus
2) Data bus
3) Control & status signals
4) Power supply signals
5) Clock signals
6) Interrupts & externally initiated signals
7) Serial I/O signals

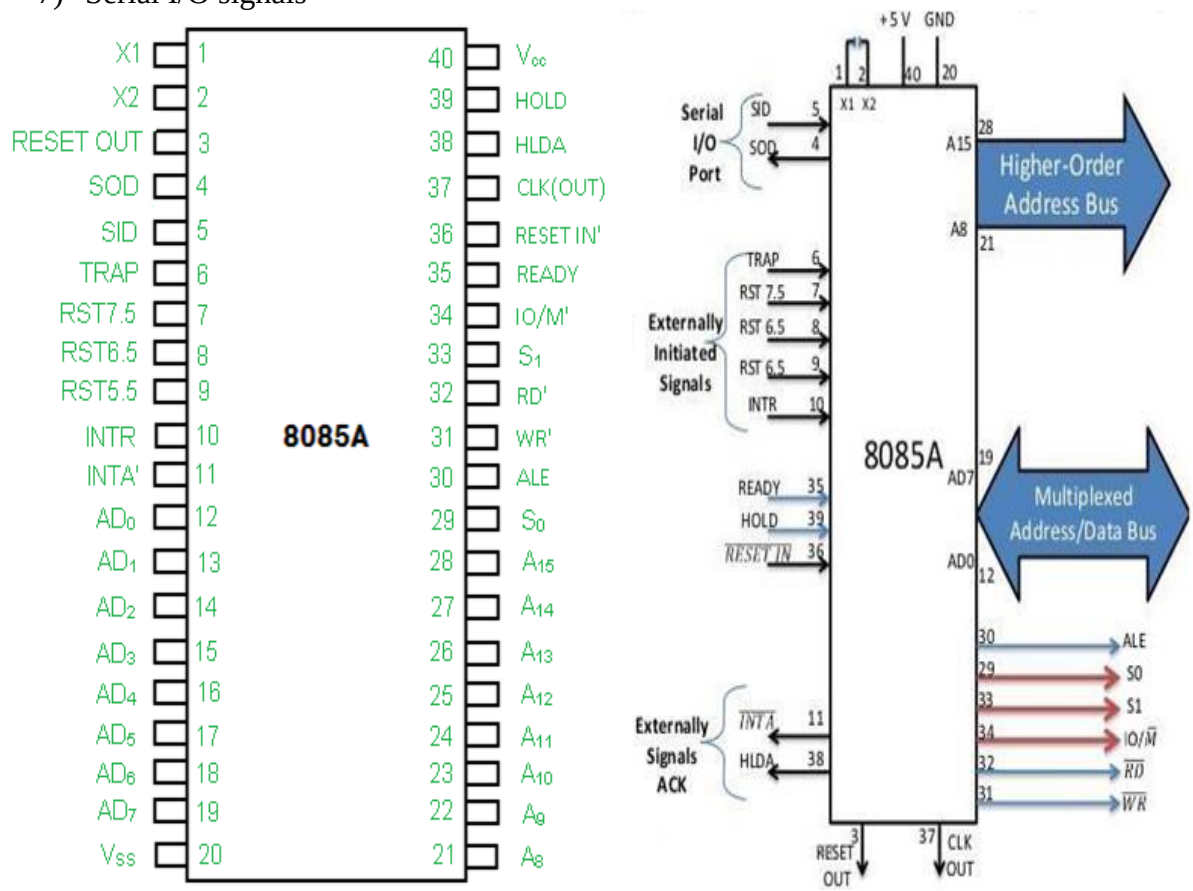

Figure: Pin diagram of 8085 microprocessor

ADDRESS BUS: A_{15}-A_8, it carries the most significant 8-bits of memory/IO address.

DATA BUS: AD_7-AD_0, it carries the least significant 8-bit address and data bus.

CONTROL AND STATUS SIGNALS: These signals are used to identify the nature of operation. There are 3 control signal and 3 status signals.

• Three **control signals** are RD, WR & ALE.
RD − This signal indicates that the selected IO or memory device is to be read and is ready for accepting data available on the data bus.
WR −This signal indicates that the data on the data bus is to be written into a selected memory or IO location.
ALE − It is a positive going pulse generated when a new operation is started by the microprocessor. When the pulse goes high, it indicates address. When the pulse goes down it indicates data.

• Three **status signals** are IO/M, S_0 & S_1:
IO/M: This signal is used to differentiate between IO and Memory operations, i.e. when it is high indicates IO operation and when it is low then it indicates memory operation.
S_1 & S_0: These signals are used to identify the type of current operation.

S_1	S_0	Operation
0	**0**	HALT
0	**1**	WRITE
1	**0**	READ
1	**1**	FETCH

POWER SUPPLY SIGNALS: There are 2 power supply signals − V_{CC} & V_{SS}. V_{CC} indicates +5v power supply and V_{SS} indicates ground signal.

CLOCK SIGNALS: There are 3 clock signals, i.e. X_1, X_2, CLK OUT.
X_1, X_2 − A crystal (RC, LC N/W) is connected at these two pins and is used to set frequency of the internal clock generator. This frequency is internally divided by 2.
CLK OUT −This signal is used as the system clock for devices connected with the microprocessor.

INTERRUPTS & EXTERNALLY INITIATED SIGNALS: Interrupts are the signals generated by external devices to request the microprocessor to perform a task. There are 5 interrupt signals, i.e. TRAP, RST 7.5, RST 6.5, RST 5.5, and INTR.

INTA − It is an interrupt acknowledgment signal.
Reset In −This signal is used to reset the microprocessor by setting the program counter to zero.
Reset Out −This signal is used to reset all the connected devices when the microprocessor is reset.
Ready −This signal indicates that the device is ready to send or receive data. If READY is low, then the CPU has to wait for READY to go high.
HOLD −This signal indicates that another master is requesting the use of the address and data buses.
HLDA (HOLD Acknowledge) − It indicates that the CPU has received the HOLD request and it will relinquish the bus in the next clock cycle. HLDA is set to low after the HOLD signal is removed.

SERIAL I/O SIGNALS: There are 2 serial signals, i.e. SID and SOD and these signals are used for serial communication.
SOD (Serial output data line) −The output SOD is set/reset as specified by the SIM instruction.
SID (Serial input data line) −The data on this line is loaded into accumulator whenever a RIM instruction is executed.

ARCHITECTURE OF 8085

The 8085A is a complete 8 bit parallel central processor. It requires a single +5 volt supply. Its basic clock speed is 3 MHz thus improving on the present 8080's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU, a RAM/ IO, and a ROM or PROM/IO chip.

The 8085A uses a multiplexed Data Bus. The address is split between the higher 8bit Address Bus and the lower 8bit Address/Data Bus. During the first cycle the address is sent out. The lower 8bits are latched into the peripherals by the Address Latch Enable (ALE). During the rest of the machine cycle the Data Bus is used for memory or l/O data.

The 8085A provides RD, WR, and IO/Memory signals for bus control. An Interrupt Acknowledge signal (INTA) is also provided. Hold, Ready, and all Interrupts are synchronized. The 8085A also provides serial input data (SID) and serial output data (SOD) lines for simple serial interface.

In addition to these features, the 8085A has three maskable, restart interrupts and one non-maskable trap interrupt. The 8085A provides RD, WR and IO/M signals for Bus control. The architecture of 8085 and functional description of each block is given below.

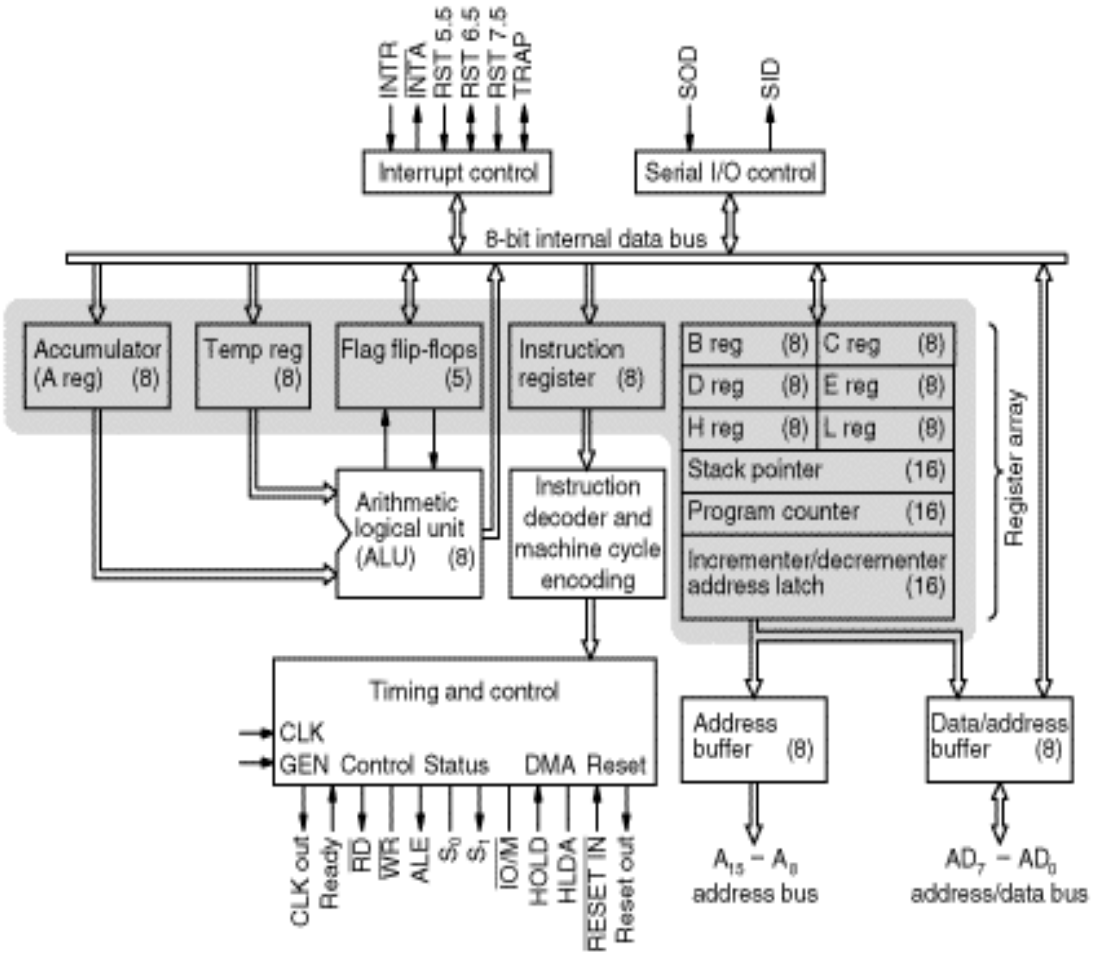

Figure: Architecture of 8085

Instruction register and decoder:
It is an 8-bit register. When an instruction is fetched from memory then it is stored in the Instruction register. Instruction decoder decodes the information present in the Instruction register.

Timing and control unit:
It provides timing and control signal to the microprocessor to perform operations. Following are the timing and control signals, which control external and internal circuits −

- Control Signals: READY, RD', WR', ALE
- Status Signals: S0, S1, IO/M'
- DMA Signals: HOLD, HLDA
- RESET Signals: RESET IN, RESET OUT

Interrupt control:
As the name suggests it controls the interrupts during a process. When a microprocessor is executing a main program and whenever an interrupt occurs, the microprocessor shifts the control from the main program to process the incoming request. After the request is completed, the control goes back to the main program.

There are 5 interrupt signals in 8085 microprocessor: INTR, RST 7.5, RST 6.5, RST 5.5 and TRAP.

Serial Input/output control:
It controls the serial data communication by using these two instructions: SID (Serial input data) and SOD (Serial output data).

Address buffer and address-data buffer:
The content stored in the stack pointer and program counter is loaded into the address buffer and address-data buffer to communicate with the CPU. The memory and I/O chips are connected to these buses; the CPU can exchange the desired data with the memory and I/O chips.

Address bus and data bus:
Data bus carries the data to be stored. It is bidirectional, whereas address bus carries the location to where it should be stored and it is unidirectional. It is used to transfer the data & Address I/O devices.

Arithmetic and logic unit:
It performs arithmetic and logical operations like Addition, Subtraction, AND, OR, etc. on 8-bit data.

Register organization:
Accumulator: It is an 8-bit register used to perform arithmetic, logical, I/O & LOAD/STORE operations. It is connected to internal data bus & ALU.

General purpose registers: There are 6 general purpose registers in 8085 processor, i.e. B, C, D, E, H & L. Each register can hold 8-bit data. These registers can work in pair to hold 16-bit data and their pairing combination is like B-C, D-E & H-L.

Program counter: It is a 16-bit register used to store the memory address location of the next instruction to be executed. Microprocessor increments the program whenever an instruction is

being executed, so that the program counter points to the memory address of the next instruction that is going to be executed.

Stack pointer: It is also a 16-bit register works like stack, which is always incremented/decremented by 2 during push & pop operations.

Temporary register: It is an 8-bit register, which holds the temporary data of arithmetic and logical operations.

The 8085 microprocessor uses an Incrementer/Decrementer Address Latch to modify the program counter (PC) or stack pointer (SP) values. This 16-bit register allows the microprocessor to increment or decrement the address stored in these registers, which is essential for sequential instruction fetching and stack operations.

BUS TIMING AND INSTRUCTION TIMING

The working of 8085 microprocessor can best be understood by considering the timing diagrams of its few instructions. The graphical representation depicting the necessary steps carried out in a machine cycle is known as **Timing Diagram**. As is well known that the total time required for the execution of an instruction is the time required to fetch and execute an instruction.

Instruction Cycle = Instruction fetch + Instruction execution

The instruction cycle may be of one, two or three bytes. During the fetch cycle, an instruction of the program (op code) is extracted from the memory locations and copied in the instruction register (IR) of CPU. The op code of the instruction copied in the instruction register (IR) is decoded during the execution cycle to perform the specific activities.

Timing diagram:

The time required by the microprocessor to complete an operation of accessing memory or input/output devices is called **machine cycle**. One time period of frequency of microprocessor is called **t-state**. A t-state is measured from the falling edge of one clock pulse to the falling edge of the next clock pulse. Fetch cycle takes four t-states and execution cycle takes three t-states.

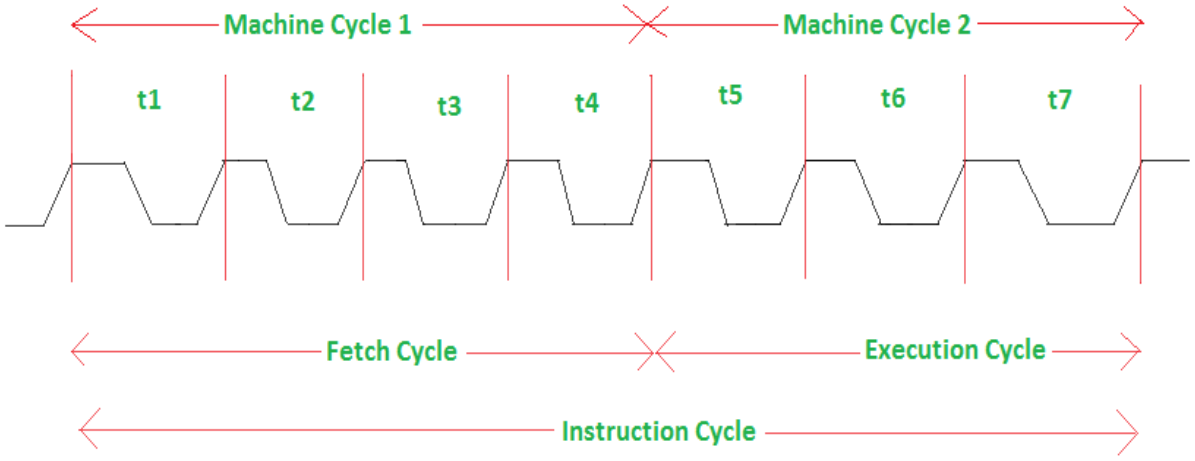

Figure: Instruction cycle of 8085

The 8085 microprocessor has 5 basic machine cycles. They are

- Opcode fetch cycle (4T)
- Memory read cycle (3 T)
- Memory write cycle (3 T)
- I/O read cycle (3 T)
- I/O write cycle (3 T)

Timing diagram for fetch cycle or op-code fetch:

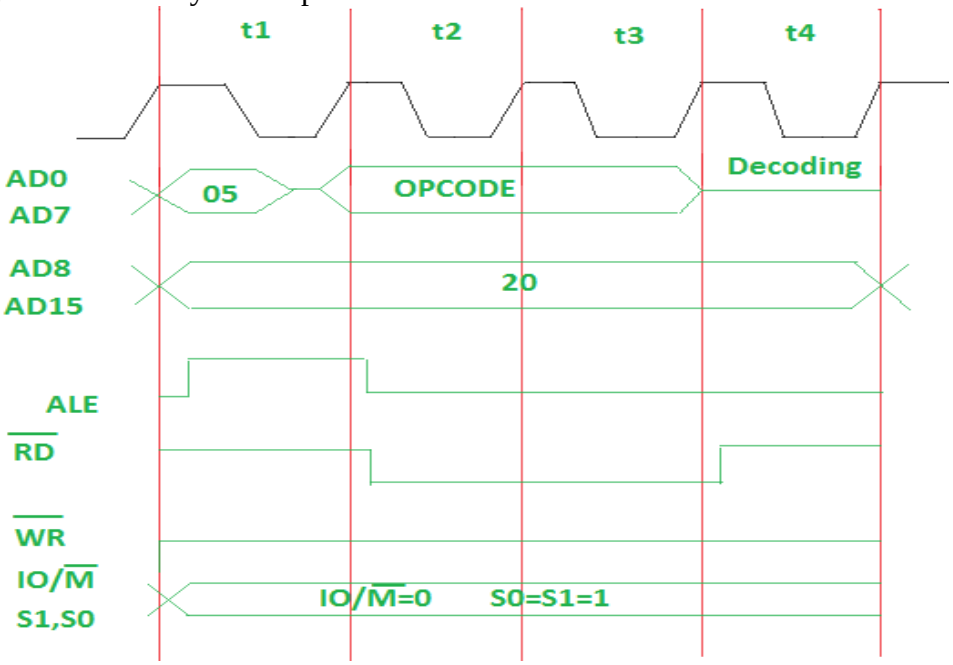

Figure: Timing diagram for opcode fetch

Above diagram represents:

05 –lower bit of address where opcode is stored. Multiplexed address and data bus AD_0-AD_7 are used.

20 –higher bit of address where opcode is stored. Multiplexed address and data bus AD_8-AD_{15} are used.

ALE –Provides signal for multiplexed address and data bus. If signal is high or 1, multiplexed address and data bus will be used as address bus. To fetch lower bit of address, signal is 1 so that multiplexed bus can act as address bus. If signal is low or 0, multiplexed bus will be used as data bus. When lower bit of address is fetched then it will act as data bus as the signal is low.

RD (low active) –If signal is high or 1, no data is read by microprocessor. If signal is low or 0, data is read by microprocessor.

WR (low active) –If signal is high or 1, no data is written by microprocessor. If signal is low or 0, data is written by microprocessor.

IO/M (low active) and S_1, S_0 –If signal is high or 1, operation is performing on input output. If signal is low or 0, operation is performing on memory.

Table: 8085 machince cycle status and control signals

Machine Cycle	Status			Control Signals		
	IO/$\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
Opcode Fetch	0	1	1	0	1	1
Memory Read	0	1	0	0	1	1
Memory Write	0	0	1	1	0	1
I/0 Read	1	1	0	0	1	1
I/O Write	1	0	1	1	0	1
Interrupt Acknowledge	1	1	1	1	1	0
HALT	Z	0	0	Z	Z	1
HOLD	Z	X	X	Z	Z	1
RESET	Z	X	X	Z	Z	1

Where Z is tri state (pin neither connected to supply nor ground. High impedance) and X represents do not care.

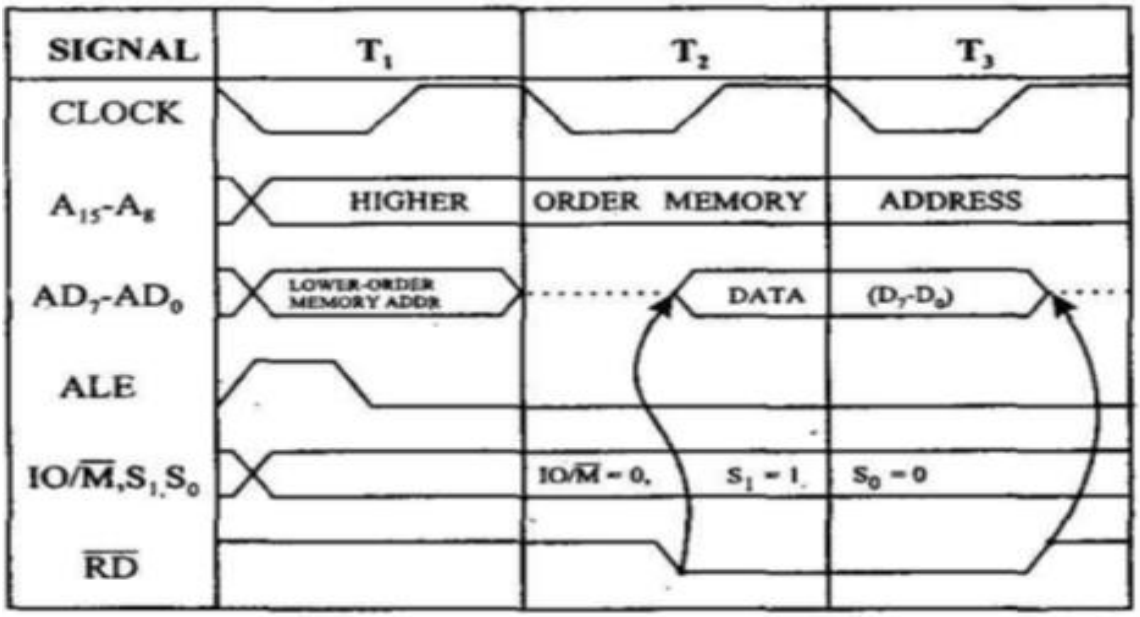

Figure: Memory read timing diagram

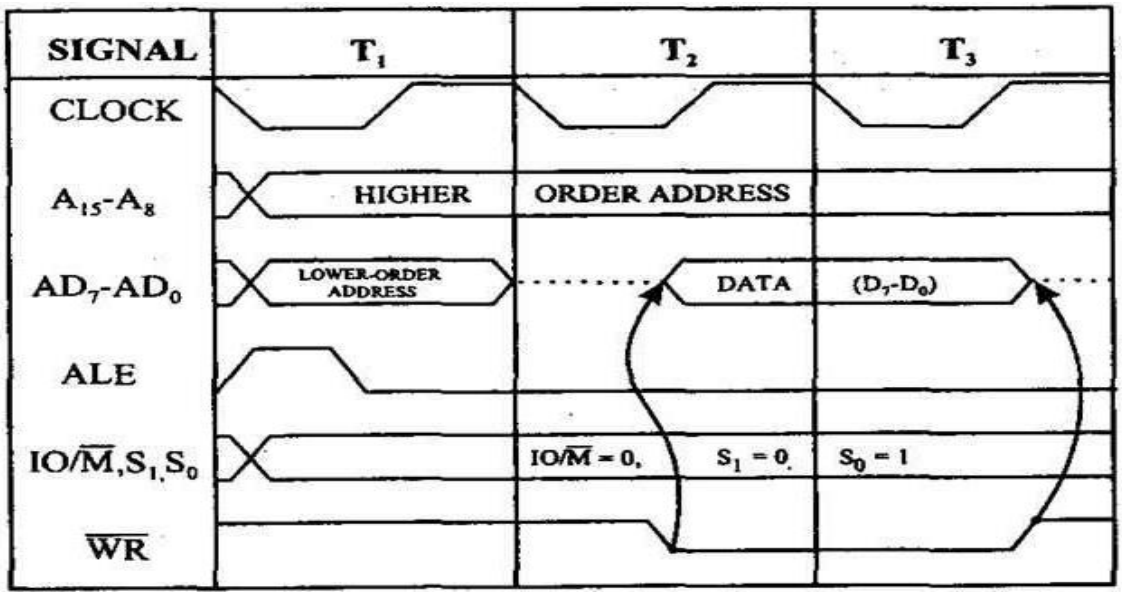

Figure: Memory write timing diagram

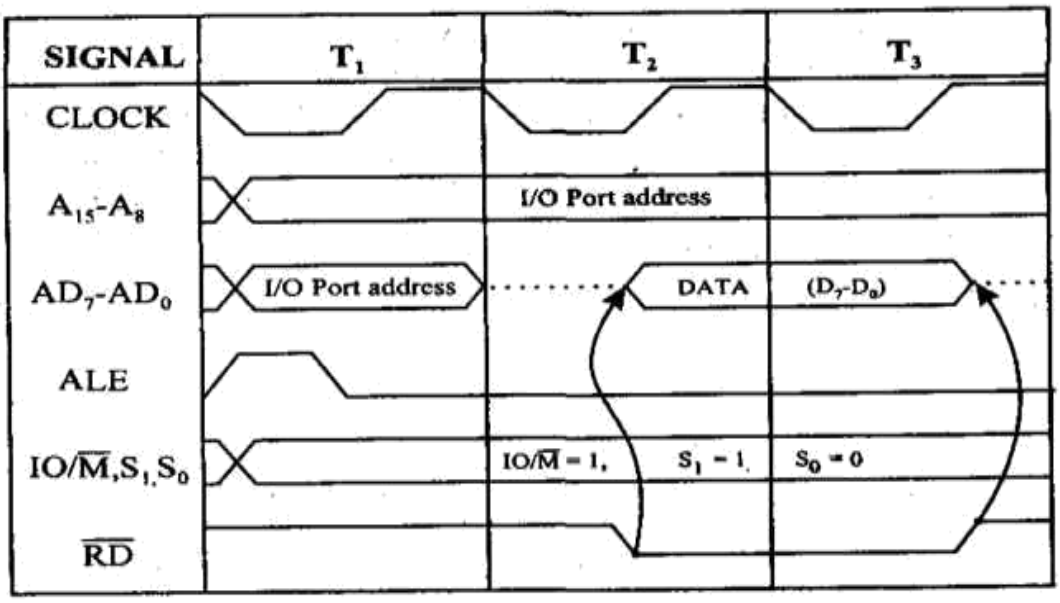

Figure: I/O read timing diagram

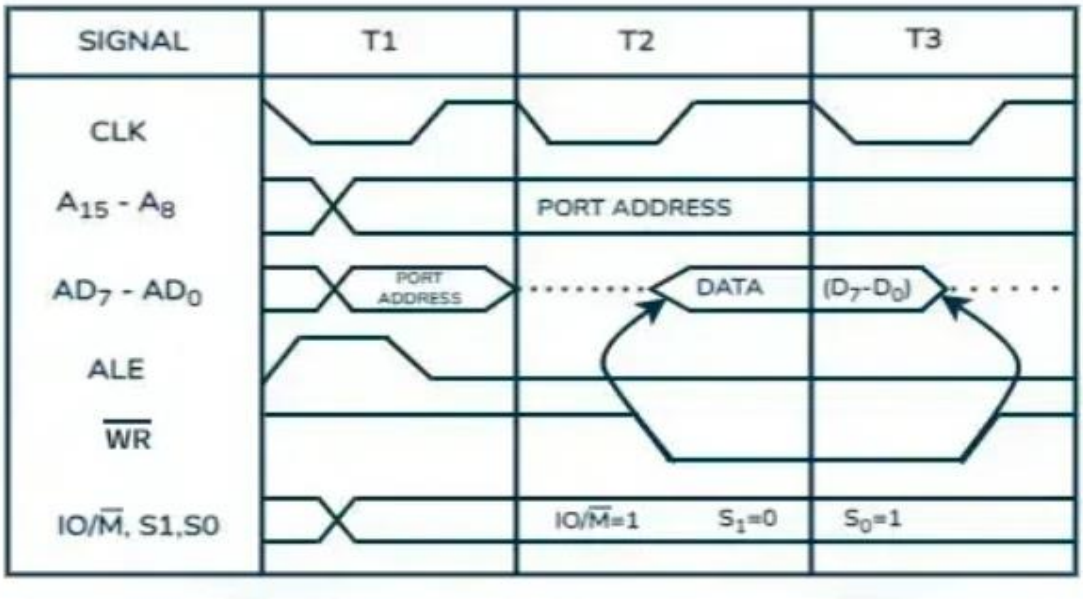

Figure: I/O write timing diagram

Timing Diagram of *MOV reg, M*

The timing diagram of the instruction ***MOV reg, M*** is shown in the below figure. This is an indirect read instruction and takes two memory cycles (M_1 and M_2). The **first** machine cycle (M_1) is known as **instruction fetch cycle**, during which the op code of the instruction is fetched from the memory. This machine cycle takes four T- states. The **second** machine cycle M_2 is known as the **execution cycle** during which the data from the memory location addressed by H-L register pair is transferred to the given register. The second machine takes three states.

During the first T-state (T_1) of M_1 cycle, microprocessor sends the address of the memory location where the op code of the instruction ***MOV reg, M*** is stored, to the address lines. The high order byte of the PC (PCH) is placed on A_8-A_{15} lines and it stays on till T_4. The low order byte of PC (PCL) is placed on the address data lines (AD_0-AD_7) which stays on only during T_1-state. For this purpose ALE (Address Latch Enable) signal gives a positive pulse midway through first T-state (T_1), which latches the low order byte.

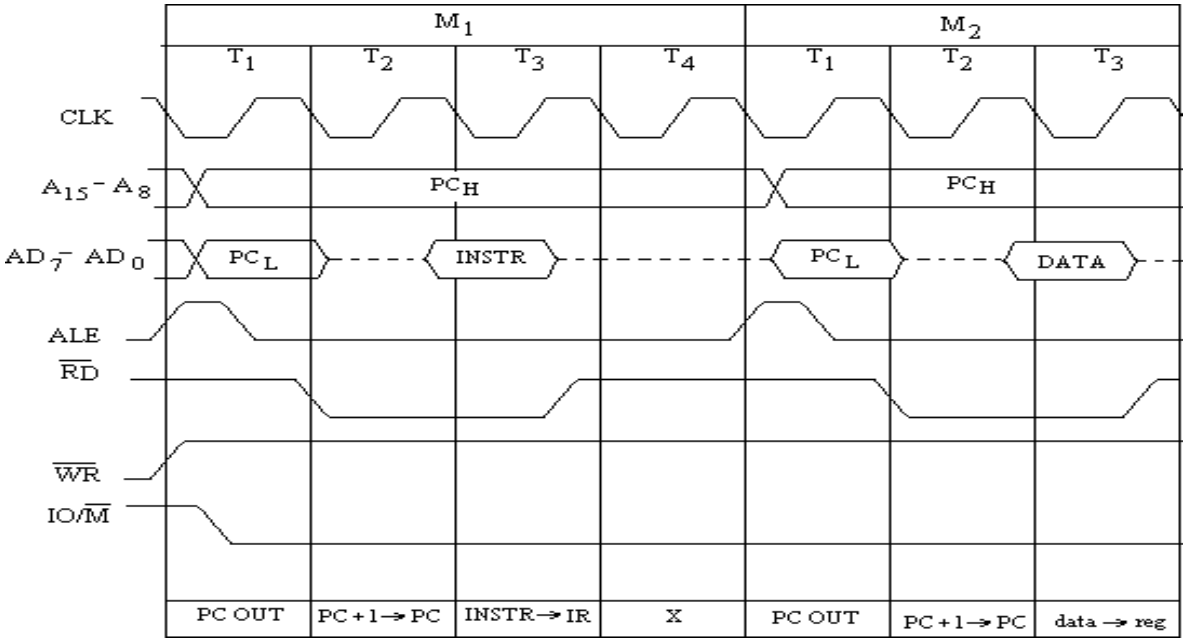

Figure: Timing Diagram of *MOV reg, M*

During the second T-state (T_2) of this op code fetch cycle, program counter (PC) is incremented (PC = PC + 1). The address disappears from the address data bus (AD_7- AD_0) at the beginning of T_2 state. This is shown by dashed line indicating the data on the bus is invalid or meaningless. At the beginning of T_2 state *RD* signal goes low and remains low till the middle of the T_3 state.

During the third T-state (T_3) of M_1 machine cycle, the op code of the instruction is read out from the memory which is sent to the instruction register (IR) i.e. *INSTR → IR*. The fourth T-state (T_4) of M1 machine cycle is denoted by **X** which indicates that this T-state is needed for the instruction decoding and other internal operations before the execution cycle.

Now the second machine cycle M_2 known as execution cycle starts. During the first T-state of this execution cycle the contents of H-L register pair are placed on the address bus and address data bus. Basically, it performs the same operation as the T_1-state of M_1 cycle. During T_2 and T_3 states of M_2 machine cycle the data is read from the memory and copied in the specified register.

This completes the instruction ***MOV reg, M***. It may be noted that this instruction needs two machine cycles with 7 T-states.

Timing Diagram of *MOV M, reg*

This is an indirect write instruction. The timing diagram of MOV M, reg instruction is shown in the below figure. The first three states of memory fetch cycle M_1 are **the same as for *MOV reg, M***. During fourth T-state (T_4) of M_1, the contents of specified register are copied in the temporary register.

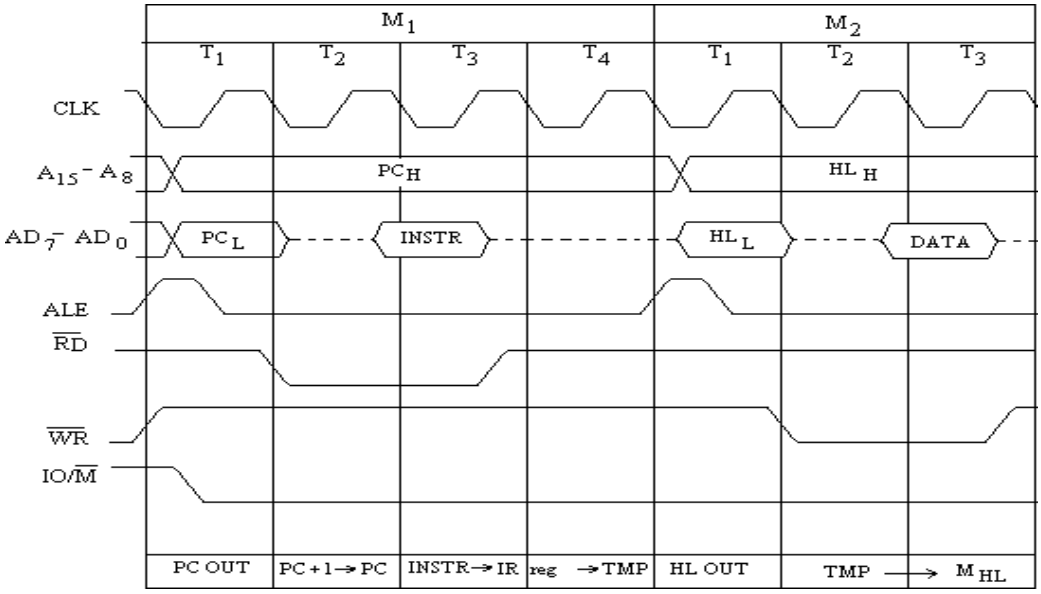

Figure: Timing Diagram of *MOV M, reg*

During the T_1-state of second machine cycle M_2, the contents of H-L pair are placed on the address and address data bus. As usual during this state ALE sends a high pulse. During T_2 and T_3 states of machine cycle M_2, contents of temporary register are transferred (copied) to the specified address. Since it is memory write instruction, so at the beginning of T_2-state *WR* signal activates (becomes low) and it remains low till half way through its T_3-state. This instruction also takes two machine cycles with 7 T-state.

FLAG REGISTER OF 8085

The ALU includes five flip-flops, which are set or reset after an operation according to data condition of the result in the accumulator and other registers. They are called Zero (Z), Carry (CY), Sign (S), Parity (P) and Auxiliary Carry (AC) flags. Their bit positions in the flag register are shown in the below figure. The microprocessor uses these flags to test data conditions.

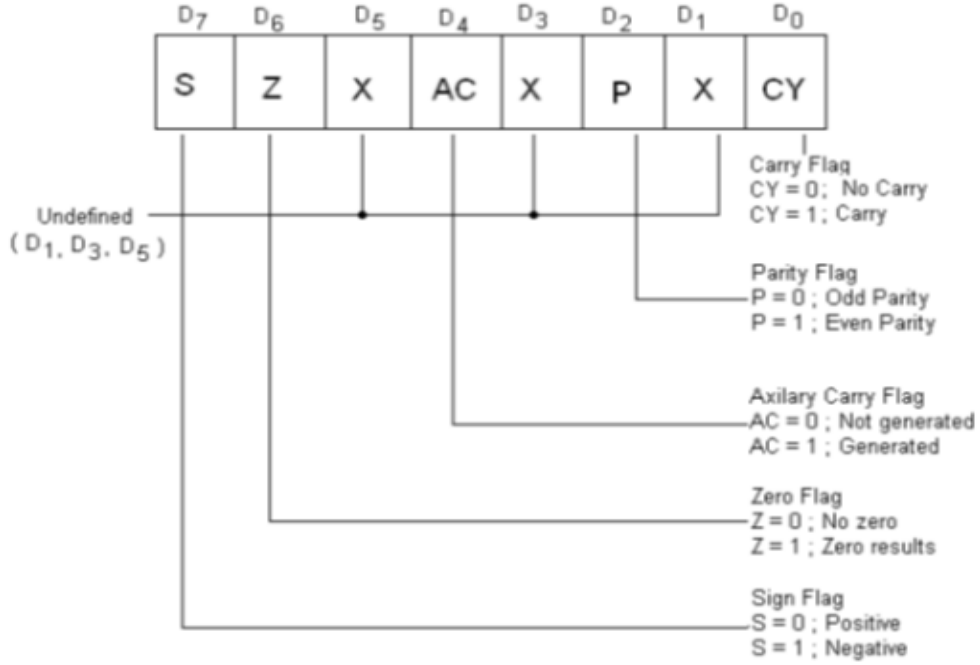

Figure: Flag register of 8085

Carry flag (CY): If arithmetic operation result in a carry. This flag is set. Carry flag also serves as a borrow flag for subtraction.

Parity flag (P): The flag along with the result provides odd parity.

Auxiliary flag (AC): It is carry generated by digit D_3 and passed onto digit D_4. Flag is used only internally for BCD operations and is not available for programmer to check and use in jump instruction.

Zero flag (Z): If an ALU operation result is zero, flag is set, else reset.

Sign flag (S): After execution of arithmetic or logic operation, bit in D_7 of result (usually accumulator). This flag is used for signed numbers. D_7 as 1, the number is negative, 0 the number is positive. Irrelevant for unsigned numbers.

PSW (Program Status Word) = Accumulator + Flag register

DE-MULTIPLEXING OF BUSES

The 8085 microprocessor has 16 address lines and 8 data lines. The address bus has 8 signal lines A_8 –A_{15} which are unidirectional. The other 8 address bits are multiplexed (time shared) with the 8 data bits. So, the bits AD_0 –AD_7 are bi-directional and serve as A_0 –A_7 and D_0 –D_7 at the same time. During the execution of the instruction, these lines carry the address bits during the early part, then during the late parts of the execution, they carry the 8 data bits.

In order to separate the address from the data, we can use a latch to save the value before the function of the bits changes. The AD_7–AD_0 lines are serving a dual purpose and that they need to be demultiplexed to get all the information.

The high order bits of the address remain on the bus for three clock periods. However, the low order bits remain for only one clock period and they would be lost if they are not saved externally. Also, notice that the low order bits of the address disappear when they are needed most.

To make sure we have the entire address for the full three clock cycles, we will use an external latch to save the value of AD_7–AD_0 when it is carrying the address bits. We use the ALE signal to enable this latch.

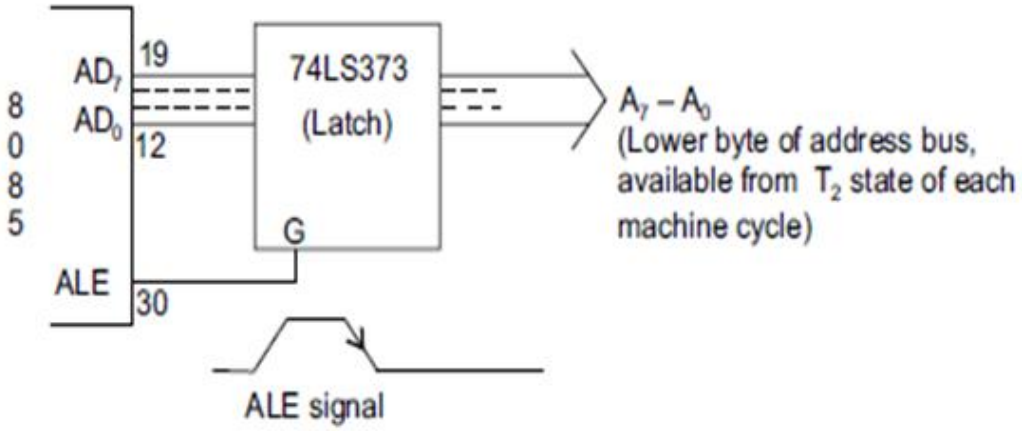

Figure: Demultiplexing of the bus AD0-AD7

Given that ALE operates as a pulse during T_1, we will be able to latch the address. Then when ALE goes low, the address is saved and the AD_7–AD_0 lines can be used for their purpose as the bi-directional data lines.

GENERATION OF CONTROL SIGNALS

Functions of Control Pins:

• IO/M' –It is a status signal which determines whether the address is for input-output or memory. When it is high (Logic 1) the address on the address bus is for input-output devices. When it is low (Logic 0) the address on the address bus is for the memory.

• RD' –It is a signal to control READ operation. When it is low the selected memory or input-output device is read.

• WR' –It is a signal to control WRITE operation. When it goes low the data on the data bus is written into the selected memory or I/O location.

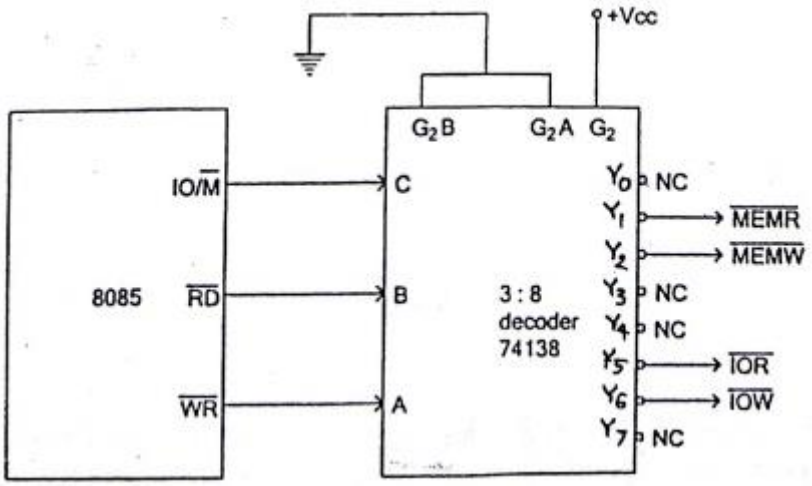

Figure: Generation of control signals of 8085

3:8 Decoder:

A 3 to 8 line decoder IC 74138 is used. It has 3-inputs and 8-outputs. Three signals from the 8085 microprocessor namely read (RD'), write (WR') and Input Output/Memory (IO/M') are connected as input to the decoder. Four output signals are taken from output pins of decoder.

Control Signals:

• S1, S0 – These are status signals. They distinguish the various types of operations such as halt, reading, instructions fetching or writing.

• RD', WR' – Read and write are two basic control signals for reading and writing operations respectively.

Functions of the control signals:

• MEMR' – It indicates Memory Read operation

• MEMW' – It indicates Memory Write operation

• IOR' – It indicates Input Read operation

• IOW' – It indicates Output Write operation

ADDRESSING MODES OF 8085

The process of specifying the data to be operated on by the instruction is called addressing. The various formats for specifying operands are called addressing modes.
The 8085 has the following five types of addressing:
1. Immediate addressing
2. Memory direct addressing
3. Register direct addressing
4. Indirect addressing
5. Implicit addressing

Immediate Addressing:

In this mode, the operand given in the instruction - a byte or word – transfers to the destination register or memory location.
Ex: MVI A, 9AH

- The operand is a part of the instruction.
- The operand is stored in the register mentioned in the instruction.

Memory Direct Addressing:

Memory direct addressing moves a byte or word between a memory location and register. The memory location address is given in the instruction.
Ex: LDA 850FH
This instruction is used to load the content of memory address 850FH in the accumulator.

Register Direct Addressing:

Register direct addressing transfer a copy of a byte or word from source register to destination register.
Ex: MOV B, C
It copies the content of register C to register B.

Indirect Addressing:

Indirect addressing transfers a byte or word between a register and a memory location.
Ex: MOV A, M
Here the data is in the memory location pointed to by the contents of HL pair. The data is moved to the accumulator.

Implicit Addressing:

In this addressing mode the data itself specifies the data to be operated upon.
Ex: CMA
The instruction complements the content of the accumulator. No specific data or operand is mentioned in the instruction.

INTERRUPTS

An interrupt is considered to be an emergency signal. The microprocessor should respond to it as soon as possible. When the microprocessor receives an interrupt signal, it suspends the currently executing program and jumps to an Interrupt Service Routine (ISR) to respond to the incoming interrupt. Each interrupt will most probably have its own ISR.

Responding to Interrupts

Responding to an interrupt may be immediate or delayed depending on whether the interrupt is **maskable or non-maskable** and whether interrupts are being masked or not. There are two ways of redirecting the execution to the ISR depending on whether the interrupt is

vectored or non-vectored. The vector is already known to the microprocessor. The device will have to supply the vector to the microprocessor

8085 Interrupts

The maskable interrupt process in the 8085 is controlled by a single flip flop inside the microprocessor. This Interrupt Enable flip flop is controlled using the two instructions Enable interrupt **"EI"** and Disable interrupt **"DI".**

The 8085 has a single Non-Maskable interrupt. The non-maskable interrupt is not affected by the value of the Interrupt Enable flip flop.

The 8085 has 5 interrupt inputs. The INTR input. The INTR input is the only non-vectored interrupt. INTR is maskable using the EI/DI instruction pair. RST 5.5, RST 6.5, RST 7.5 are all automatically vectored. RST 5.5, RST 6.5, and RST 7.5 are all maskable.

TRAP is the only **non-maskable interrupt** in the 8085 and also **automatically vectored**

Table: 8085 interrupts

Interrupt	Interrupt vector address	Maskable or non-maskable	Edge or level triggered	priority
TRAP	0024H	Non-makable	Level	1
RST 7.5	003CH	Maskable	Rising edge	2
RST 6.5	0034H	Maskable	Level	3
RST 5.5	002CH	Maskable	Level	4
INTR	Decided by hardware	Maskable	Level	5

Summary

Interrupt is a process where an external device can get the attention of the microprocessor. The process starts from the I/O device and is asynchronous.

Interrupts can be classified into two types:

- Maskable (can be delayed)
- Non-Maskable(cannot be delayed)

Interrupts can also be classified into:

- Vectored (the address of the service routine is hard-wired)
- Non-vectored (the address of the service routine needs to be supplied externally)